TMC1175A/TMC1275

Video A/D Converter

8 bit, 50 Msps

Features

- 8-Bit resolution
- 50 Msps conversion rate
- Low power: 100mW at 20 Msps
- Integral track/hold
- Integral and differential linearity error 0.5 LSB
- Single or dual +5 Volt supplies
- Differential phase 0.5 degree
- Differential gain 1.5%
- Three-state TTL/CMOS-compatible outputs
- Low cost

Applications

- Video digitizing
- VGA and CCD digitizing
- LCD projection panels
- Image scanners
- Personal computer video boards
- Multimedia systems
- Low cost, high speed data conversion

Description

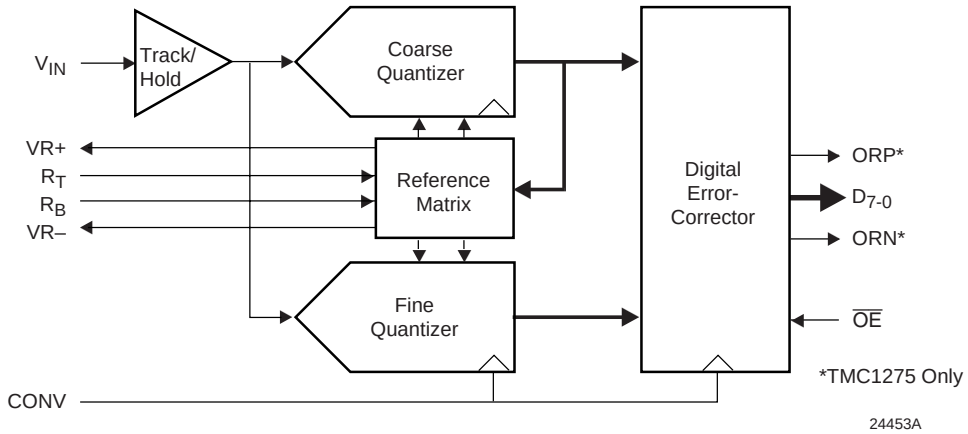
The TMC1175A/1275 analog-to-digital (A/D) converter employs a two-step flash architecture to convert analog signals into 8-bit digital words at sample rates of up to 50 Msps (Megasamples per second). An integral Track/Hold circuit delivers excellent performance on signals with full-scale frequency components up to 12 MHz. Innovative architecture and submicron CMOS technology limit typical power dissipation to 100 mW.

Power may be derived from either single or dual +5V supplies. Internal voltage reference resistors allow self-bias operation. Input capacitance is very low, simplifying or eliminating input driving amplifiers. All digital three-state outputs are TTL- and CMOS-compatible.

The TMC1175A and TMC1275 share their core architectures; the TMC1275 adds two overrange outputs that indicate when the analog input signal is beyond the conversion range.

The TMC1175A/1275 is available in 24-pin plastic DIP, 24-lead plastic SOIC, and 28-lead J-lead PLCC packages. Performance specifications are guaranteed from -20°C to 75°C.

Block Diagram



Functional Description

The TMC1175A/1275 8-bit A/D converter uses a two-step architecture to perform analog-to-digital conversion at rates up to 50 Msps. The input signal is held in an integral track/hold stage during the conversion process. Operation is pipelined, with one input sample taken and one output word provided for each CONVert cycle.

The first step in the conversion process is a coarse 4-bit quantization. This determines the range of the subsequent fine 4-bit quantization step. To eliminate spurious codes, the fine 4-bit A/D quantizer output is gray-coded and converted to binary before it is combined with the coarse result to form a complete 8-bit result.

Analog Input and Voltage References

The TMC1175A/1275 converts analog signals in the range R_B to R_T into digital data. Input signals outside that range produce “saturated” 00h or FFh output codes. The device will not be damaged by signals within the range A_{GND} to V_{DDA}.

The A/D converter input range is very flexible and extends from the +5 Volt power supply to ground. The nominal input range is 2 Volts, from 0.6V to 2.6V. The circuit is characterized and performance is specified over that range. However, the part will work well with a full-scale range from 1.0V to 5.0V. A reduced input range may simplify analog signal conditioning circuitry, at the expense of additional noise sensitivity and some reduced differential linearity performance. Similarly, increasing the range can improve differential linearity, but puts a greater burden on the input signal conditioning circuitry.

In many applications, external voltage reference sources are connected to the R_T and R_B pins. R_B can be grounded. Gain and offset errors are directly related to the accuracy and stability of the applied reference voltages.

Two reference pull-up and pull-down resistors connected to VR+ and VR– are provided internally for operation without external voltage reference circuitry (Figure 1). The reference voltages applied to R_T and R_B may be generated by connecting VR+ to R_T and VR- to R_B. The power supply voltage is divided by the on-chip resistors to bias the R_T and R_B points. This sets-up the converter for operation in its nominal range from 0.6V to 2.6V.

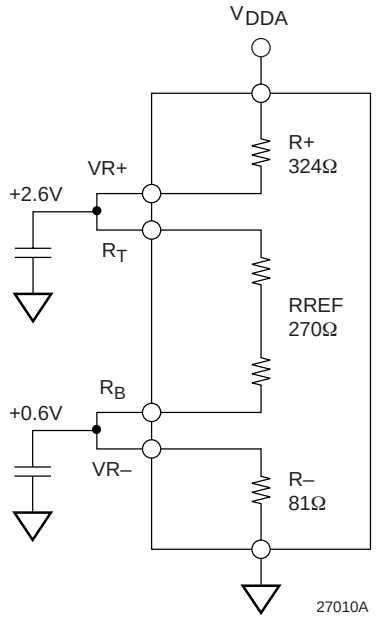


Figure 1. Reference Resistors

With V_{DDA} at 5.0V, connecting VR+ to R_T and grounding R_B will provide an input range from 0.0V to 2.27V, while connecting R_T to V_{DDA} and R_B to VR- produces a full scale range of 3.85V referenced to V_{DDA}. External resistors may also be employed to provide arbitrary reference voltages, but they will not match the temperature coefficient of the on-chip resistors as well as R+ and R-, and will cause the converter transfer function to vary with temperature.

With this implementation, errors in the power supply voltage end up on the conversion data output.

Because a two-step conversion process is employed, it is important that the references remain stable during the ENTIRE conversion process (two clock cycles). The reference voltage can then be changed, but any conversion in progress during a reference change is invalid.

Table 1. Output Coding

Input Voltage	ORP[2]	ORN[2]	Output
R_T + 1 LSB	1	0	FF
R_T	0	0	FF
R_T – 1 LSB	0	0	FE
• • •	• • •	• • •	• • •
R_B + 128 LSB	0	0	80
R_B + 127 LSB	0	0	7F
• • •	• • •	• • •	• • •
R_B + 1 LSB	0	0	01
R_B	0	0	00
R_B – 1 LSB	0	1	00

Notes:
1. LSB = (R_T – R_B) / 255
2. TMC1275 Only

Digital Inputs and Outputs

Sampling of the applied input signal takes place on the **falling** edge of the CONV signal (Figure 2). The output word is delayed by 2 1/2 CONV cycles. It is then available after the **rising** edge of CONV. The previous data on the output remain valid for t_{HO} (Output Hold Time), satisfying any hold time requirement of the receiving circuit. The new data become valid t_{DO} (Output Delay Time) after this rising edge of CONV.

Whenever the analog input signal is sampled and found to be at a level beyond the A/D conversion range, an Overrange output of the TMC1275 will go HIGH. If the input is more positive (by at least one LSB) than the positive end of the range, ORP will go HIGH and D_{7-0} will be FFh. If the input is more negative (by at least one LSB) than the negative end of the range, ORN will go HIGH and D_{7-0} will be 00h.

The outputs of the TMC1175A/1275 are CMOS- and TTL-compatible, and are capable of driving four low-power Schottky TTL (54/74LS) loads. An Output Enable control, $\overline{OE}$, places the outputs in a high-impedance state when HIGH. The outputs are enabled when $\overline{OE}$ is LOW.

Power and Ground

To minimize noise injection into the analog section, V_{DDA} may be connected to a separate regulated +5 volt supply. V_{DDD} may be connected to a digital supply. Power up sequence is immaterial. Latch-up will not occur.

A_{GND} and D_{GND} pins should be connected to a common ground plane. For optimum performance treat analog and digital PWB traces as transmission lines. Route analog connections cleanly to the TMC1175A/1275. Segregate digital connections and if necessary terminate clocks to eliminate ringing. Prevent digital return currents from flowing across analog input sections of the TMC1175A/1275.

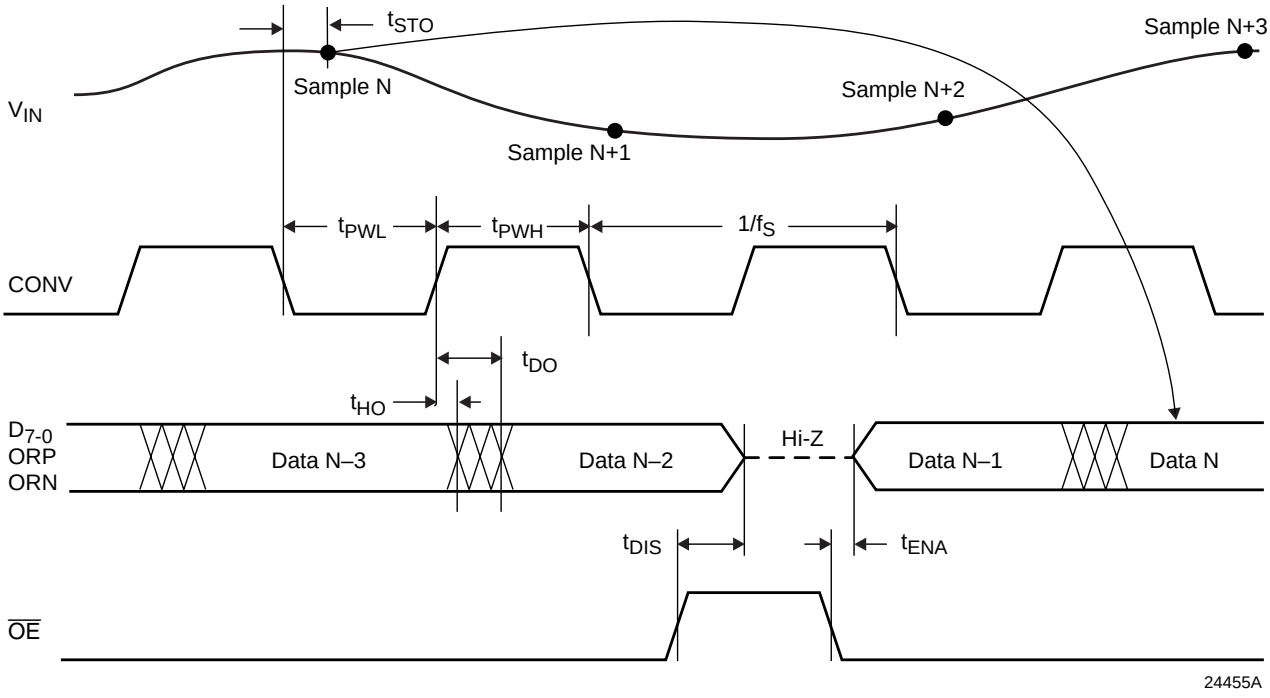


Figure 2. Conversion Timing

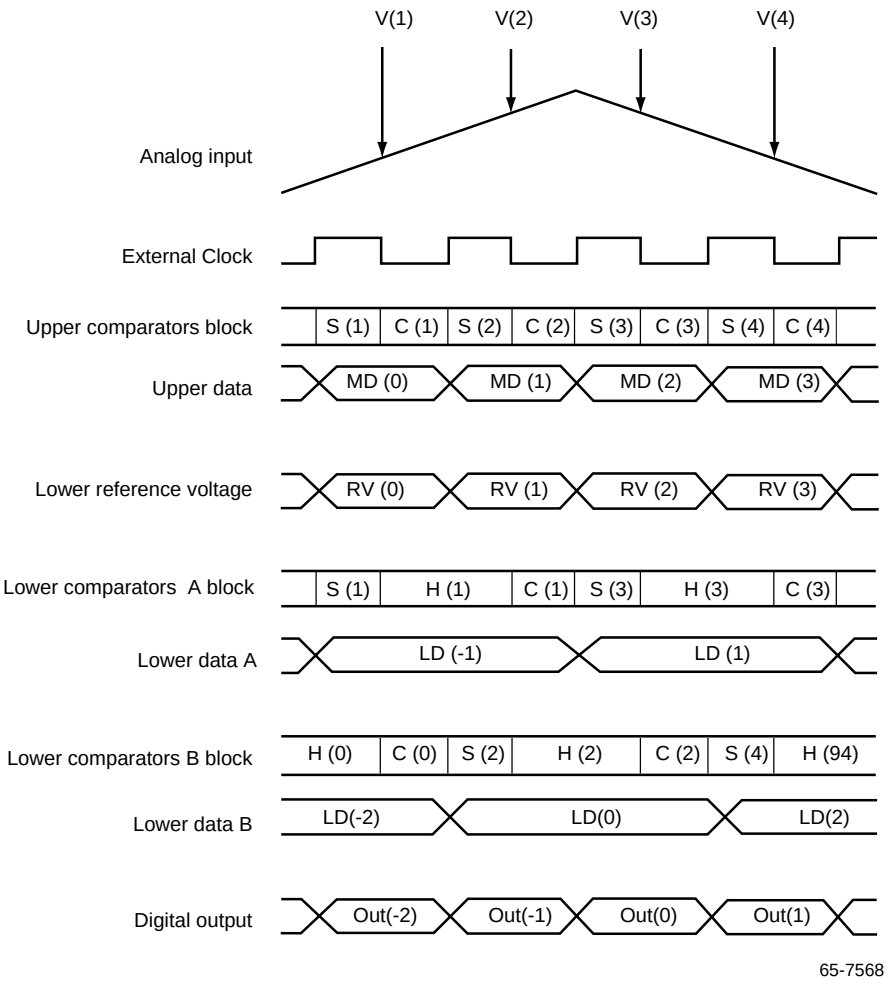
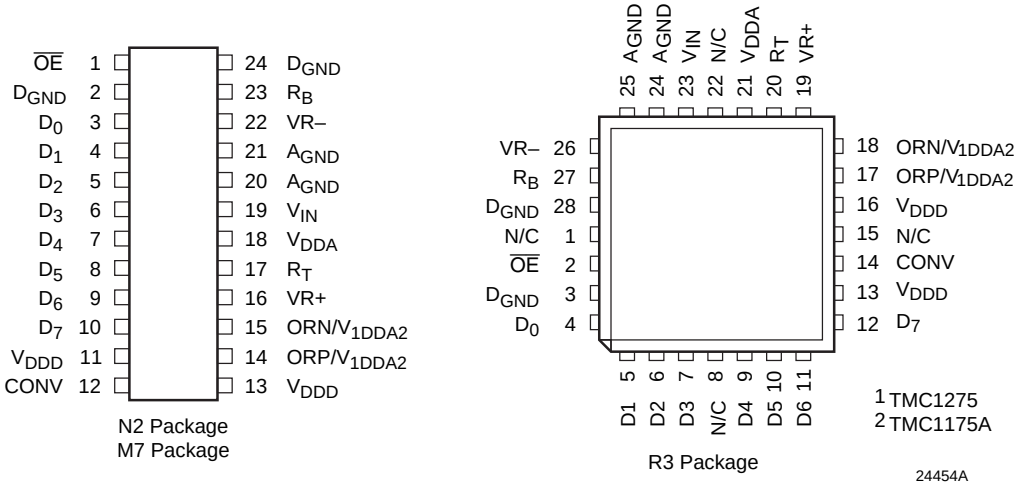


Figure 3. Internal Timing

Pin Assignments



Pin Descriptions

Pin Name	Pin Number N2, M7	Pin Number R3	Pin Type	Pin Function Description
Inputs				
V_{IN}	19	23	R_T – R_B	**Analog Input.** The input voltage conversion range lies between the voltages applied to the RT and RB pins.
R_T	17	20	2.6V	**Reference Voltage Top Input.** R_T is the top input to the reference resistor ladder. A DC voltage applied to R_T defines the positive end of the V_{IN} conversion range.
R_B	23	27	0.6V	**Reference Voltage Bottom Input.** R_B is the bottom input to the reference resistor ladder. A DC voltage applied to R_B defines the negative end of the V_{IN} conversion range.
VR+	16	19		**Reference Voltage Top Source.** VR+ is the internal pull-up reference resistor for self-bias operations.
VR–	22	26		**Reference Voltage Bottom Source.** VR- is the internal pull-down reference resistor for self-bias operations.
$\overline{OE}$	1	2	CMOS	**Output Enable.** (CMOS-compatible) When LOW, D_{7-0} are enabled. When HIGH, D_{7-0} are in a high-impedance state.
CONV	12	14	CMOS	**Convert (Clock) Input.** (CMOS-compatible) V_{IN} is sampled on the falling edge of CONV.
Outputs				
D_{7-0}	10–3	12–9, 7–4	CMOS/ TTL	**Data Outputs (D7 = MSB).** Eight-bit CMOS- and TTL-compatible digital outputs. Data is output following the rising edge of CONV.
ORP[1]	14[1]	17[1]	CMOS/ TTL	**OverRange Positive Output.** When HIGH, ORP indicates that the analog input voltage is at least one LSB higher than the voltage that produces output code FFh. ORP is synchronous with D_{7-0}.
ORN[1]	15[1]	18[1]	CMOS/ TTL	**OverRange Negative Output.** When HIGH, ORN indicates that the analog input voltage is at least one LSB lower than the voltage that produces output code 00h. ORN is synchronous with D_{7-0}.
Power				
V_{DDA}	14[2], 15[2], 18	17[2], 18[2], 21	+5V	**Analog Supply Voltage.** Independent +5 volt power connection to analog comparator circuits.
V_{DDD}	11, 13	13, 16	+5V	**Digital Supply Voltage.** Independent +5 volt power connection to digital error correction and output drivers.
A_{GND}	20, 21	24, 25	0.0V	**Analog Ground.** Connect to the system analog ground plane.
D_{GND}	2, 24	3, 28	0.0V	**Digital Ground.** Connect to the system analog ground plane.
No Connect				
N/C		1, 8, 15, 22	open	Not Connected.

Notes:

1. TMC1275 Only.
2. TMC1175A Only.

Bandwidth Specification Notes

The specification for bandwidth of an A/D converter is somewhat different from the normal frequency-response specification used in amplifiers and filters. An understanding of the differences will help in selecting converters properly for particular applications.

A/D conversion comprises two distinct processes: *sampling* and *quantizing*. *Sampling* is "grabbing" a snapshot of the input signal and holding it steady for quantizing. The *quantizing* process is approximating the analog input, which may be any value within the conversion range, with its nearest numerical value. While sampling is a high-frequency process, quantizing operates on a dc signal, held steady by the track/hold circuit. Therefore, the sampling process is what relates to the dynamic characteristics of the converter.

Sampling involves an *aperture time*, the time during which the track/hold is trying to capture the input signal and settle on a dc value to hold. It is analogous to the shutter speed of a camera: the shorter the aperture (or faster the shutter) the less the signal will be blurred, and the less uncertainty there will be in the quantized value.

For example, a 10 MHz sinewave with a 1V peak amplitude (2Vp-p) has a maximum slew rate of $2\pi fA$ at zero crossing, or 62.8V/μs. With an 8-bit A/D converter, q (the quantization step size) = 2V/255 = 7.8mV. The input signal will slew one LSB in 124ps. To limit the error (and noise) contribution due to *aperture effects* to 1/2LSB, the aperture must be shorter than 62ps.

This is the primary reason that the signal to noise ratio drops off as full scale frequency increases. Note, also, that the slew rate is directly proportional to signal amplitude, A. A/Ds will handle lower-amplitude signals of higher bandwidth.

All this is of particular interest in applications such as digitizing analog VGA RGB signals, or the output of a CCD imaging chip. These data are effectively pre-sampled: there is a period of rapid slewing from one pixel value to another, followed by a relatively stable dc level before the signal slews to the next pixel value. The goal is, of course, to sample on these pixel values, not on the slewing between pixels. During the aperture time, the A/D sees essentially a dc signal, and classic bandwidth considerations are not important. As long as the input circuit can slew and settle to the new value in the prescribed period, an accurate conversion will be made.

The TMC1175A/1275 is capable of slewing a full 2V and settling between samples taken as little as 25ns apart, making it ideal for digitizing analog VGA and CCD outputs.

Equivalent Circuits and Threshold Level

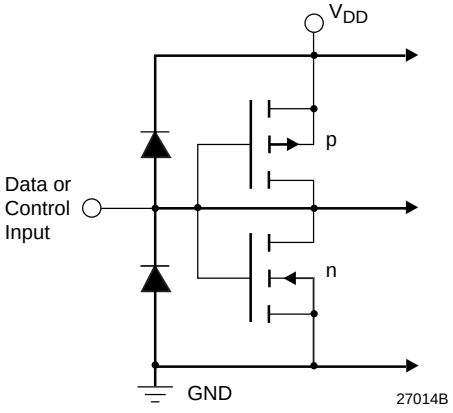


Figure 4. Equivalent Digital Input Circuit

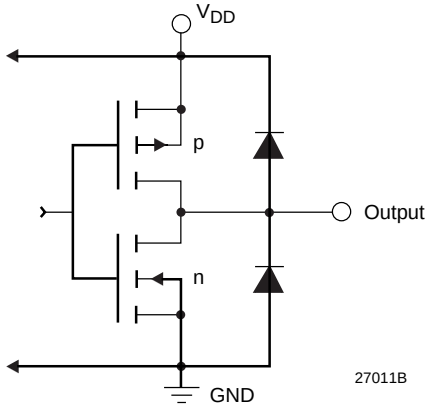


Figure 5. Equivalent Digital Output Circuit

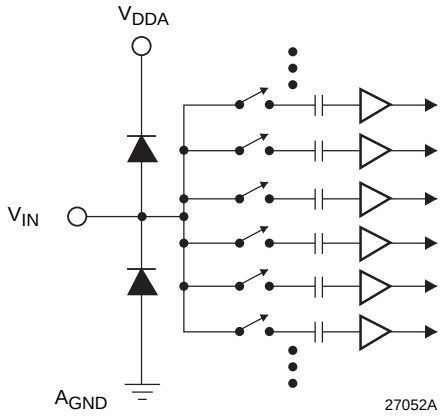


Figure 6. Equivalent Analog Input Circuit

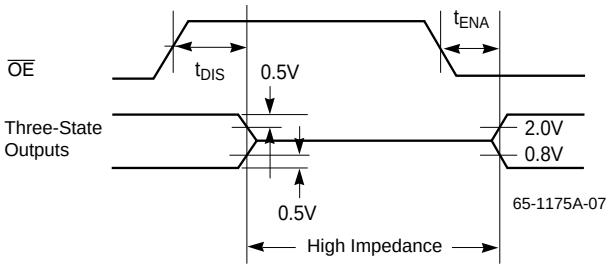


Figure 7. Threshold Levels for Three-State Measurements

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply Voltages					
V_{DDA}	Measured to A_{GND}	-0.5		7.0	V
V_{DDD}	Measured to D_{GND}	-0.5		7.0	
V_{DDA}	Measured to V_{DDD}	-0.5		0.5	V
A_{GND}	Measured to D_{GND}	-0.5		0.5	
Digital Inputs					
Applied Voltage[2]	Measured to D_{GND}	-0.5		V_{DDD} + 0.5	V
Forced Current[3,4]		-10.0		10.0	mA
Analog Inputs					
Applied Voltage[2]	Measured to A_{GND}	-0.5		V_{DDA} + 0.5	V
Forced Current[3,4]		-10.0		10.0	mA
Outputs					
Applied Voltage[2]	Measured to D_{GND}	-0.5		V_{DDD} + 0.5	V
Forced Current[3,4]		-6.0		6.0	mA
Short Circuit Duration	Single output in HIGH state to ground			1	sec
Temperature					
Operating, Ambient		-20		110	°C
Junction				150	°C
Storage		-65		150	°C
Lead Soldering	10 seconds			300	°C
Vapor Phase Soldering	1 minute			220	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DDD}	Digital Power Supply Voltage		4.75	5.0	5.25	V
V_{DDA}	Analog Power Supply Voltage		4.75	5.0	5.25	V
A_{GND}	Analog Ground (Measured to D_{GND})		-0.1	0	0.1	V
f_S	Conversion Rate	TMC1175A/1275-20			20	Msps
		TMC1175A/1275-30			30	Msps
		TMC1175A/1275-40			40	Msps
		TMC1175A/1275-50			50	Msps
t_{PWH}	CONV Pulsewidth, HIGH	TMC1175A/1275-20	15			ns
		TMC1175A/1275-30	13			ns
		TMC1175A/1275-40	12			ns
		TMC1175A/1275-50	9			ns
t_{PWL}	CONV Pulsewidth, LOW	TMC1175A/1275-20	15			ns
		TMC1175A/1275-30	12			ns
		TMC1175A/1275-40	12			ns
		TMC1175A/1275-50	9			ns
V_{RT}	Reference Voltage, Top		2.0	2.6	V_{DDA}	V
V_{RB}	Reference Voltage, Bottom		0	0.6	3.0	V
V_{RT}-V_{RB}	Reference Voltage Differential		1.0		5.0	V
V_{IN}	Analog Input Range		V_{RB}		V_{RT}	V
V_{IH}	Input Voltage, Logic HIGH		0.7 x V_{DDD}		V_{DDD}	V
V_{IL}	Input Voltage, Logic LOW		GND		0.3 x V_{DDD}	V
I_{OH}	Output Current, Logic HIGH				-4.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		-20		75	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
I_{DD}	Power Supply Current[1]	V_{DDD} = V_{DDA} = Max, C_{LOAD} = 35pF				
		f_S = 20Msps		20	30	mA
		f_S = 30Msps		25	35	mA
		f_S = 40Msps		30	40	mA
		f_S = 50Msps		35	48	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DDD} = V_{DDA} = Max				
		CONV = LOW		7	18	mA
		CONV = HIGH		10	20	mA

Electrical Characteristics (continued)

Parameter		Conditions	Min	Typ[1]	Max	Units
P_D	Total Power Dissipation	V_{DDD} = V_{DDA} = Max, C_{LOAD} = 35pF				
		f_S = 20Msps		100	160	mW
		f_S = 30Msps		125	185	mW
		f_S = 40Msps		150	210	mW
		f_S = 50Msps		185	250	mW
C_{AI}	Input Capacitance, Analog	CONV = LOW		4		pF
		CONV = HIGH		12		pF
R_{IN}	Input Resistance		500	1000		kΩ
I_{CB}	Input Current, Analog				±1	μA
R_{REF}	Reference Resistance		200	270	340	Ω
I_{IH}	Input Current, HIGH	V_{DDD} = Max, V_{IN} = V_{DDD}			±5	μA
I_{IL}	Input Current, LOW	V_{DDD} = Max, V_{IN} = 0V			±5	μA
I_{OZH}	Hi-Z Output Leakage	V_{DDD} = Max, V_{IN} = V_{DDD}			±5	μA
I_{OZL}	Hi-Z Output Leakage	V_{DDD} = Max, V_{IN} = 0V			±5	μA
I_{OS}	Short-Circuit Current				-30	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = -100μA	V_{DDD}-0.3			V
		I_{OH} = -2.5mA	3.5			V
		I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V
C_{DI}	Digital Input Capacitance			4	10	pF
C_{DO}	Digital Output Capacitance			10		pF

Note:

1. Typical values with V_{DDD} = V_{DDA} = Nom and T_A = Nom, Minimum/Maximum values with V_{DDD} = V_{DDA} = Max and T_A = Min.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{STO}	Sampling Time Offset		2	5	8	ns
t_{HO}	Output Hold Time	C_{LOAD} = 15pF	5			ns
t_{DO}	Output Delay Time	C_{LOAD} = 15pF			20	ns
t_{ENA}	Output Enable Time				27	ns
t_{DIS}	Output Disable Time				42	ns

System Performance Characteristics

Parameter		Conditions	Min	Typ[1]	Max	Units
E_{LI}	Integral Linearity Error, Independent	V_{RT} = 2.6V V_{RB} = 0.6V		±0.5	±1	LSB
E_{LD}	Differential Linearity Error	V_{RT} = 2.6V V_{RB} = 0.6V		±0.3	±1	LSB
BW	Bandwidth[2]	TMC1175A/1275-20 TMC1175A/1275-30 TMC1175A/1275-40 TMC1175A/1275-50			10 12 12 12	MHz MHz MHz MHz
E_{AP}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	R_T – V_{IN} for most positive code transition	-8	-25	-42	mV
E_{OB}	Offset Voltage, Bottom	R_B – V_{IN} for most negative code transition	30	40	60	mV
dg	Differential Gain	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} = 2.6V, V_{RB} = 0.6V		1.5	2.7	%
dp	Differential Phase	f_S = 14.3Msps NTSC 40 IRE Mod Ramp V_{DDA} = +5.0V, T_A=25°C V_{RT} = 2.6V, V_{RB} = 0.6V		0.5	1.0	deg
SNR[3]	Signal-to-Noise Ratio	f_S = 20Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 1.24MHz	44	48		dB
		f_{IN} = 2.48MHz	43	47		dB
		f_{IN} = 6.98MHz	41	45		dB
		f_{IN} = 10.0MHz	37	42		dB
		f_S = 30Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 1.24MHz	42	47		dB
		f_{IN} = 2.48MHz	40	45		dB
		f_{IN} = 6.98MHz	38	43		dB
		f_{IN} = 10.0MHz	33	39		dB
		f_{IN} = 12.0MHz	30	37		dB
		f_S = 40Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 1.24MHz	40	45		dB
		f_{IN} = 2.48MHz	38	43		dB
		f_{IN} = 6.98MHz	36	41		dB
		f_{IN} = 10.0MHz	34	38		dB
		f_{IN} = 12.0MHz	32	36		dB
		f_S = 50Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 10.0MHz	30			dB

System Performance Characteristics (continued)

Parameter		Conditions	Min	Typ[1]	Max	Units
SFDR[4]	Spurious-Free Dynamic Range	f_S = 20Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 1.24MHz	46	52		dB
		f_{IN} = 2.48MHz	44	51		dB
		f_{IN} = 6.98MHz	41	45		dB
		f_{IN} = 10.0MHz	38	43		dB
		f_S = 30Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 1.24MHz	42	49		dB
		f_{IN} = 2.48MHz	40	45		dB
		f_{IN} = 6.98MHz	37	41		dB
		f_{IN} = 10.0MHz	35	40		dB
		f_{IN} = 12.0MHz	34	39		dB
		f_S = 40Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 1.24MHz	40	44		dB
		f_{IN} = 2.48MHz	39	43		dB
		f_{IN} = 6.98MHz	38	41		dB
		f_{IN} = 10.0MHz	36	40		dB
		f_{IN} = 12.0MHz	36	39		dB
		f_S = 50Msps, V_{RT} = 2.6V, V_{RB} = 0.6V				
		f_{IN} = 10.0MHz	33			dB

Notes:

1. Values shown in Typ column are typical for V_{DDD} = V_{DDA} = +5V and T_A = 25°C.
2. Bandwidth is the frequency up to which a full-scale sinewave can be digitized without spurious codes.
3. SNR values do not include the harmonics of the fundamental frequency.
4. SFDR is the ratio in dB of fundamental amplitude to the harmonic with the highest amplitude.

Typical Performance Characteristics

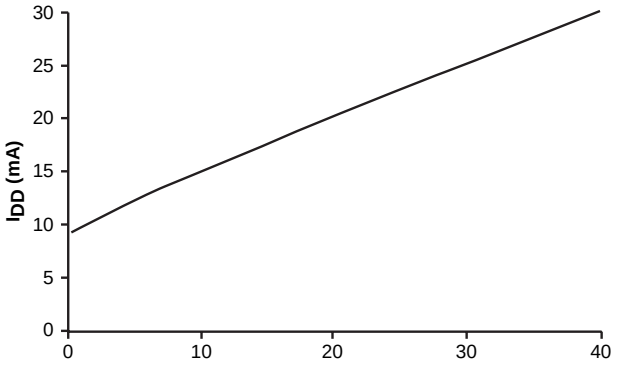


Figure 8. Typical I_{DD} vs f_S

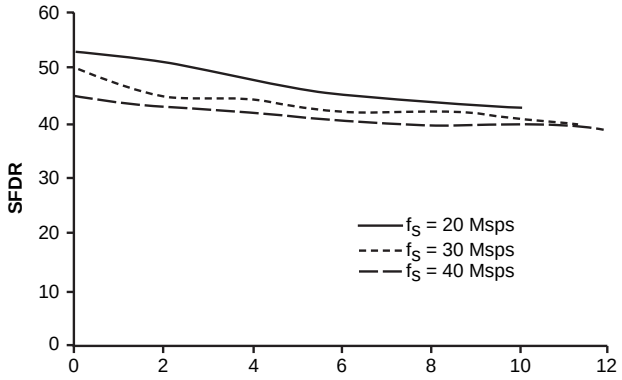


Figure 9. Typical SFDR vs f_{IN} and f_S

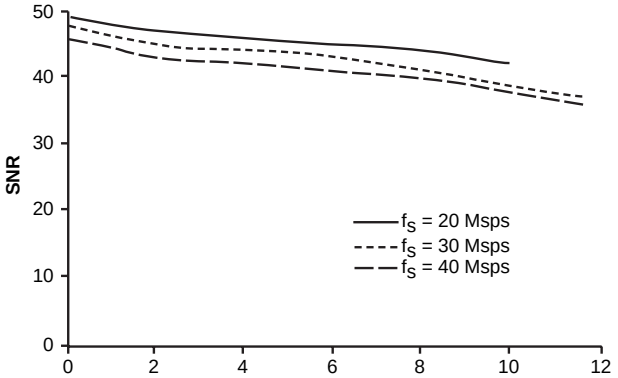


Figure 10. Typical SNR vs f_{IN} and f_S

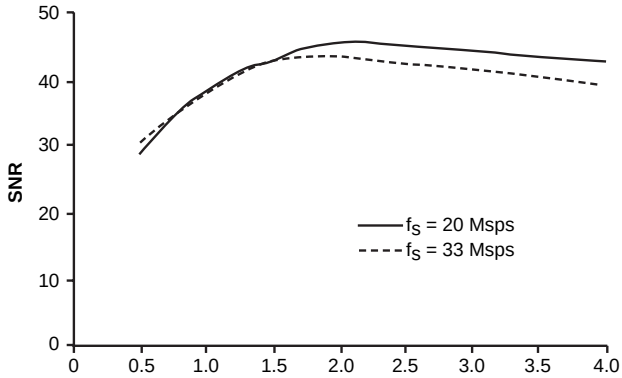


Figure 11. Typical SNR vs Full Scale Input Range

Applications Discussion

The circuit in Figure 12 employs a band-gap reference to generate a variable RT reference voltages for the TMC1175A/1275 as well as a bias voltage to offset the wideband input amplifier to mid-range. An "offset adjust" is also shown for varying the mid-range voltage level. The operational amplifier in the reference circuitry is a standard 741-type.

The voltage reference at R_T can be adjusted from 0.0 to 2.4 volts while R_B is grounded. Diodes are used to restrict the wideband amplifier output to between -0.7V and V_{DD} +0.7V. Diode protection is good practice to limit the analog input voltage at V_{IN} to the safe operating range.

The circuit in Figure 13 shows self-bias of R_T and R_B by connection to VR+ and VR-. This sets up a 0.6 to 2.6 Volt input range for V_{IN}. The input range is susceptible to power supply variation since the voltages on R_T and R_B are directly derived from V_{DDA}. The video input is AC-coupled and biased at a adjustable midpoint of the A/D input range. This circuit offers the advantage of minimum support circuitry for the most cost-sensitive applications.

In Figure 14, an external band-gap reference sets R_T to +1.2 Volts while R_B is grounded. The internal pull-up resistor, R+, provides the bias current for the band-gap reference. The A/D converter input is biased to the mid-point of the input range.

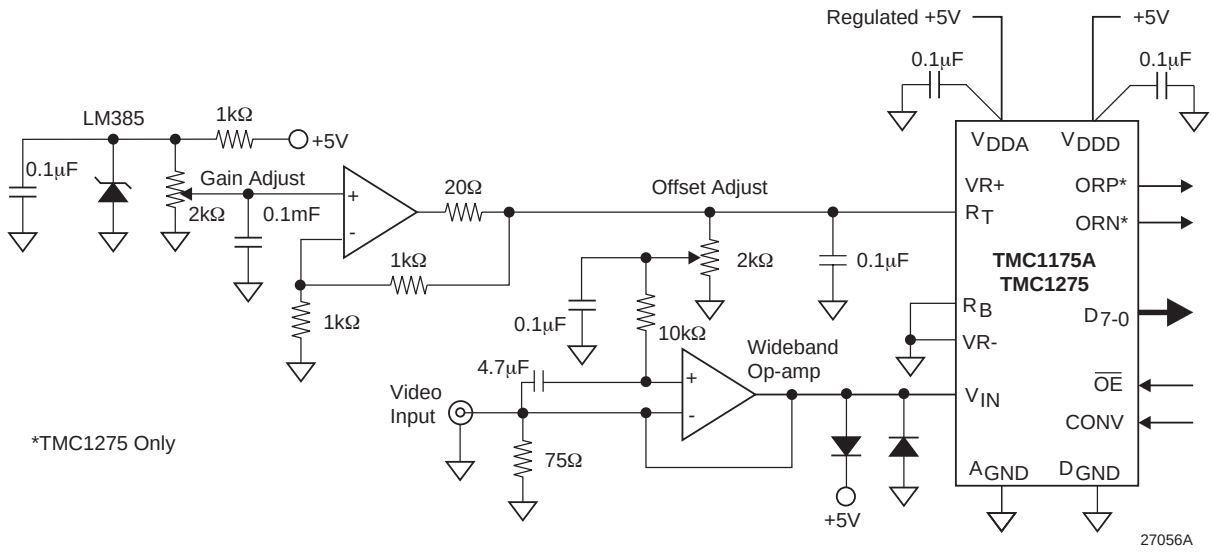


Figure 12. Typical Interface Circuit - High Performance

Grounding

The TMC1175A/1275 has separate analog and digital circuits. To keep digital system noise from the A/D converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) originate from separate sources with V_{DDA} regulated, and that ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin. The digital circuitry that gets its input from the TMC1175A/1275 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option, even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{IN}, R_T, R_B, VR+, VR-) as short as possible and as far as possible from all digital signals. The TMC1175A/1275 should be located near the board edge, close to the analog input connectors.

2. The power plane for the TMC1175A/1275 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1175A/1275 is the same as that of the system's digital circuitry, power to the TMC1175A/1275 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

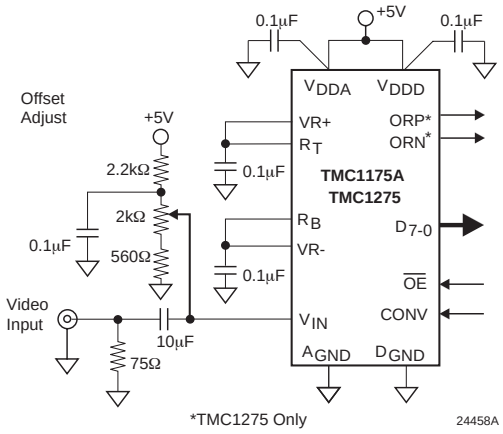


Figure 13. Typical Interface Circuit – Low Cost

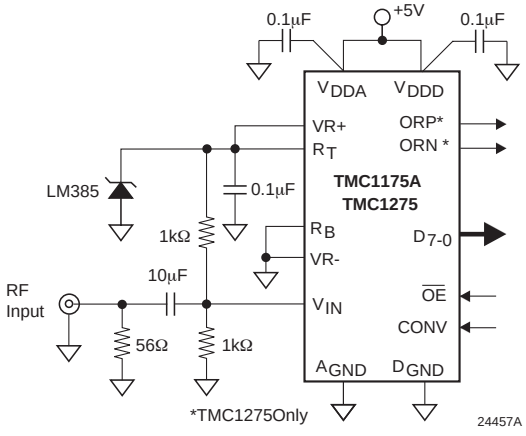


Figure 14. Typical Interface Circuit – Stabilized Reference

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1μF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC1175A/1275, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1175A/1275 and its related analog circuitry can have an adverse effect on performance.

6. CONV should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line at the CONV input, if required, to eliminate overshoot and ringing.

Evaluation Board

An evaluation board is available that implements good interface practices and provide a convenient testbed for developing system applications and circuit variations. An on-board D/A converter is provided to reconstruct the digitized signal and to evaluate converter performance.

Contact your sales representative for information.

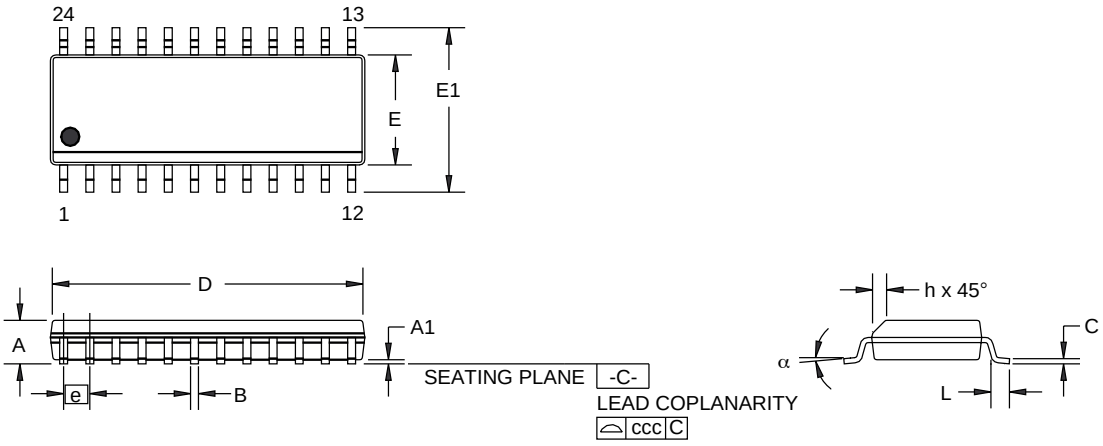
Notes:

Notes:

Mechanical Dimensions

24 Lead SOIC (5.4 mm) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.067	.075	1.70	1.90	
A1	.004	.012	0.10	0.31	
B	.014	.020	0.36	0.51	
C	.006	.012	0.15	0.30	
D	.587	.610	14.90	15.50	
E	.205	.220	5.20	5.60	
E1	.295	.319	7.50	8.10	
e	.050 BSC		1.27 BSC		
h	.010	.020	0.25	0.50	
L	.016	.050	0.41	1.27	
N	24		24		
α°	0	8	0	8	
ccc	-	.004	-	0.10	



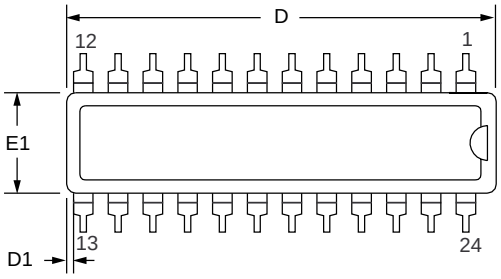
Mechanical Dimensions (continued)

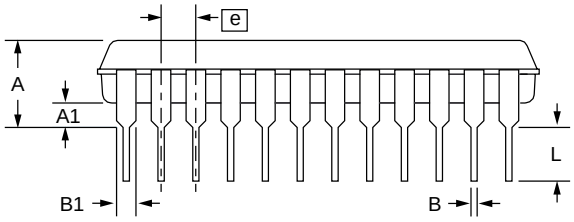
24 Lead Plastic DIP .300" Package

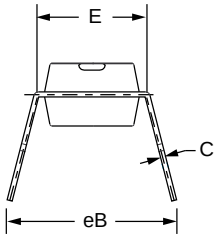
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.53	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	1.125	1.275	28.58	32.39	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	24		24		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







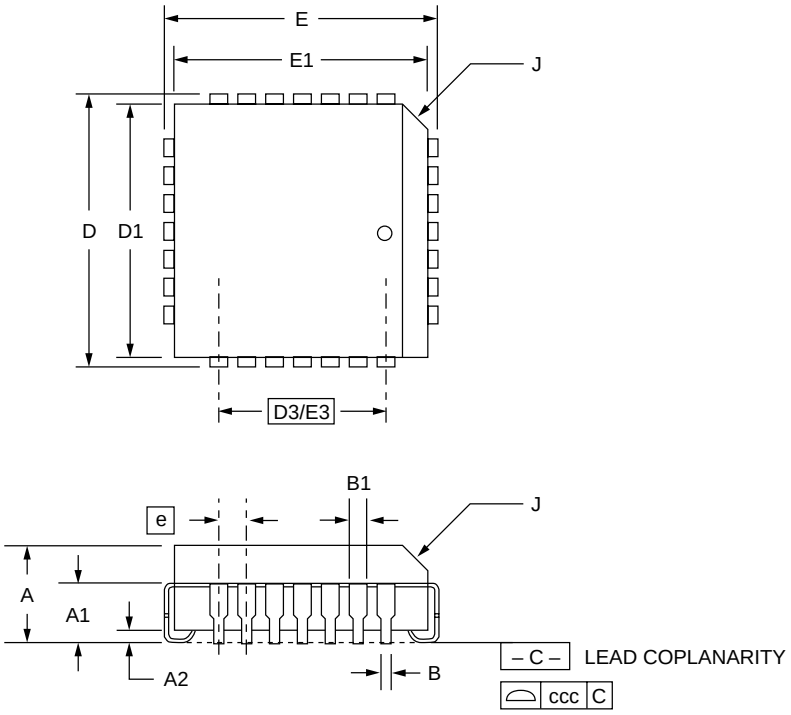
Mechanical Dimensions (continued)

28 Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Conversion Rate	Temperature Range	Screening	Package	Package Marking
TMC1175AM7C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C20
TMC1175AM7C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C30
TMC1175AM7C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C40
TMC1175AM7C50	50 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1175AM7C50
TMC1175AN2C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C20
TMC1175AN2C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C30
TMC1175AN2C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C40
TMC1175AN2C50	50 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1175AN2C50
TMC1175AR3C20	20 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C20
TMC1175AR3C30	30 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C30
TMC1175AR3C40	40 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C40
TMC1175AR3C50	50 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1175AR3C50
TMC1275M7C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C20
TMC1275M7C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C30
TMC1275M7C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C40
TMC1275M7C50	50 Msps	T_A = -20°C to 75°C	Commercial	24-Lead SOIC	1275M7C50
TMC1275N2C20	20 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C20
TMC1275N2C30	30 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C30
TMC1275N2C40	40 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C40
TMC1275N2C50	50 Msps	T_A = -20°C to 75°C	Commercial	24-Lead PDIP	1275N2C50
TMC1275R3C20	20 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C20
TMC1275R3C30	30 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C30
TMC1275R3C40	40 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C40
TMC1275R3C50	50 Msps	T_A = -20°C to 75°C	Commercial	28-Lead PLCC	1275R3C50